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Design of application specific non-linear ADC for neural signal recording in Brain Machine Interfaces

Pratibha Dwivedi, D. K. Mishra

Abstract— In the linear ADC the useful as well as the non-useful information is digitized with the same resolution. Non-linear analog to digital converter (NLADC) are designed in order to focus more on the segment where greater information is concentrated. In this work a NLADC is designed for neural signal recording to be used in biomedical sensor applications. This ADC utilizes the exponential quantization function, consolidated into linear SARADC such that the conversion is performed based on the non-linear quantization function. It is designed for 1.5 V supply voltage and implemented in 0.18 µm technology. The maximum resolution obtained is 9.7 bits and the minimum resolution is 2 bits. The clock frequency is 250 KHz. Its dynamic range is 64.1 dB, which is 15.9 dB higher than the linear ADC with 8 physical bits. It occupies an area of 0.03521 mm^2 and power dissipation of 31.04 µW has been achieved.

Index Terms— Analog to Digital converters, Binary to thermometer converter, Biomedical sensor application, Brain Machine Interfaces, non-linear ADC, op-amp, SAR logic.

1 Introduction

IN the last few years, there has been a growing interest for developing wireless sensing device for portable and implantable biomedical applications. These sensing devices are generally used for detecting and monitoring biomedical signals such as Electrocardiographic (ECG), Electroencephalography (EEG), Electromyography (EMG).

In the neuroscientific applications neural signal is recorded from hundreds of channels for analysis and signal processing. There are some major limitations for high density neural signal recording and these are bandwidth limitation and power dissipation.

Research is going on to develop various data reduction techniques. The techniques involve signal processing approaches such as discrete wavelet transform [1], [2], [3] and Walsh-Hadamard transform [4] to spike detection [5], [6] and spike sorting techniques [7]. In some techniques such as spike detection and spike sorting technique, there is loss of information which is not suitable for neuroscientific applications.

Another major concern for sensory system in biomedical application is the power dissipation; this has led researchers to develop a wide variety of techniques to reduce the power dissipation. The SAR block and DAC were replaced with the binary search algorithm in [8], DAC design has been modified in [9], split SARADC has been implemented in [10]. Particularly ADCs for implantable biomedical devices need microwatt operation to run on small batteries for decades. Therefore, energy efficiency is a critical challenge for ADCs design.

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Non-linear ADCs are extremely useful in sensing application where the input signal and the background noise are spread out over a wide dynamic range. Non-linear ADCs can be implemented in two ways, the first technique is to linearly quantize the input signal and then map the output digital code according to the non-linear quantization function [11]. In the second approach the non-linear function of interest is consolidated into analog to digital conversion process such that the conversion is based on the non-linear function [12], [13], [14]. Later technique is more efficient in terms of power and area requirements.

In this work an 8 bit application specific NLADC is designed for neural signal recording. The NLADC is designed for 1.5 volt supply and implemented in 0.18 µm technology. This ADC is designed for low power applications using voltage scaling technique and its digital blocks are implemented using transmission gate logic.

2 Exponential Quantization Function

Neural signal fall into the category of signals that have information concentrated at higher ends and for these signals the quantization function is needed, which are having increasing slope i.e., exponential quantization function. The exponential quantization function is interfused to the successive approximation analog to digital convertor in [15] to non-linearly digitize the neural signal.

$$Vin,\min = Vbl = (00....0)binary \quad (1)$$

$$Vin,\max = Vfs - LSB = (11....1)binary \quad (2)$$

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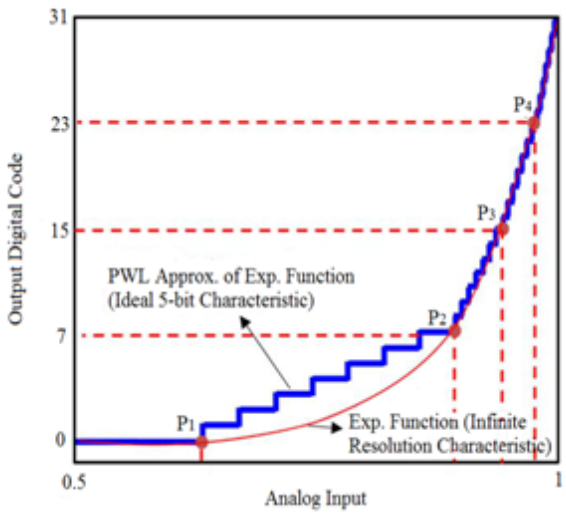
Figure 1: Piecewise linearly approximated exponential quantization function.



Vbl is the baseline voltage (nearly 0V) , *Vfs* is the full-scale input range for the ADC. The input output relationship for the exponential quantization function [15] is,

$$[(B_{N-1}2^{N-1} + ... + b_0)/2^N]$$
$$= a[\exp\{(Vin - Vbl/Vfs) \times k\} - 1] \quad (3)$$

The relationship between 'a' and 'k' is,

$$k = \ln[(1/a) + 1] \quad (4)$$

Hence, only 'a' controls the curvature of the exponential curve, the value of 'a' is 0.0019. Fig. 1 illustrates the piecewise linearly approximated exponential quantization function for 5 bit NLADC. The half range characteristics are divided into 2^S segments and each segment has M bit of resolution. The junction points [0, P_1, P_2, P_3, P_4] are on the desired exponential curve and the segments are digitized linearly. In this work S=3 and M=4.

3 Block Diagram

The NLADC uses a two step SARADC as shown in fig. 2, which works in three phases. First one is the sign detection phase, in this phase the input signal is compared with a certain threshold voltage *Vth*, which is temporarily set to the baseline voltage of the input signal.

After this comparison the MSB bit (sign bit) is determined and Vref and Vth are set according to the sign bit [15]. The second phase is the offset cancellation phase, in this phase an ordinary offset cancellation technique is applied. The third phase is the conversion phase, in this phase successive approximation algorithm first find the segment in which the input is present, encoded by $b_6b_5b_4$, in three clock cycles. These three bits are used to generate the seven bit thermometer code, which is used by segment selection block to generate two analog voltages related to the end point of the segment. An in-segment digitization occurs to determine the remaining bits, i.e., $b_3b_2b_1b_0$ in four clock cycles. At last, end of conversion signal goes high and resets the ADC, this completes one cycle of NLADC.

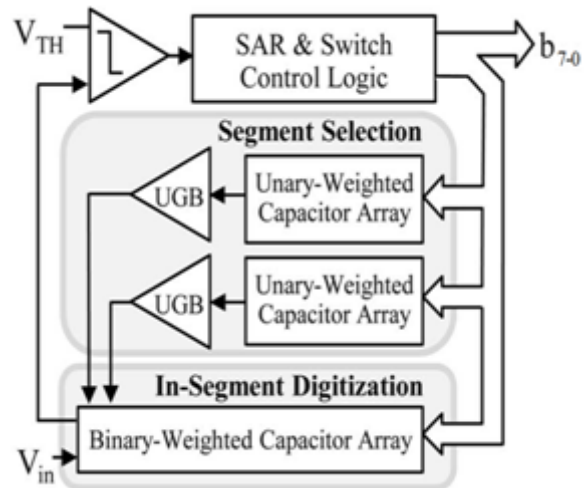


Figure 2: Block Diagram of two-step SARADC.

4 Circuit Implementation

Fig. 3 shows the circuit diagram of two-step SARADC, the circuit uses a comparator, two Unity Gain Buffers (UGB), beta reference multiplier circuit, SAR block, binary to thermometer converter, unary weighted and binary weighted metal insulator metal capacitor array and MOS switches.

The SAR block used in this work consists of a ring counter and a shift register. At least 2N flip-flops are employed in this kind of SAR [16]. For low power requirements SAR block and binary to thermometer convertor is designed using the transmission gate logic, binary to thermometer convertor when designed using CMOS logic dissipates 44.38 μW while it consumes 235.4 nW when designed using transmission gate logic at a clock frequency of 250 KHz.

Two stage op-amp is used as a comparator as shown in fig. 4, which is equipped with a frequency compensation network. The offset of the comparator is 4.36 mV. The NMOS switch disconnects the compensating capacitor in both sign detection and conversion phases in order to speed-up the operation of the comparator, this switch is closed in the offset cancellation phase to put the comparator in the unity-gain feedback configuration.

Three stage op-amp is used as UGB as shown in fig. 5; they both are biased using the beta reference multiplier circuit (fig. 4), the value of resistance used in beta reference multiplier circuit is kept high, in order to prevent the system moving towards the instability.

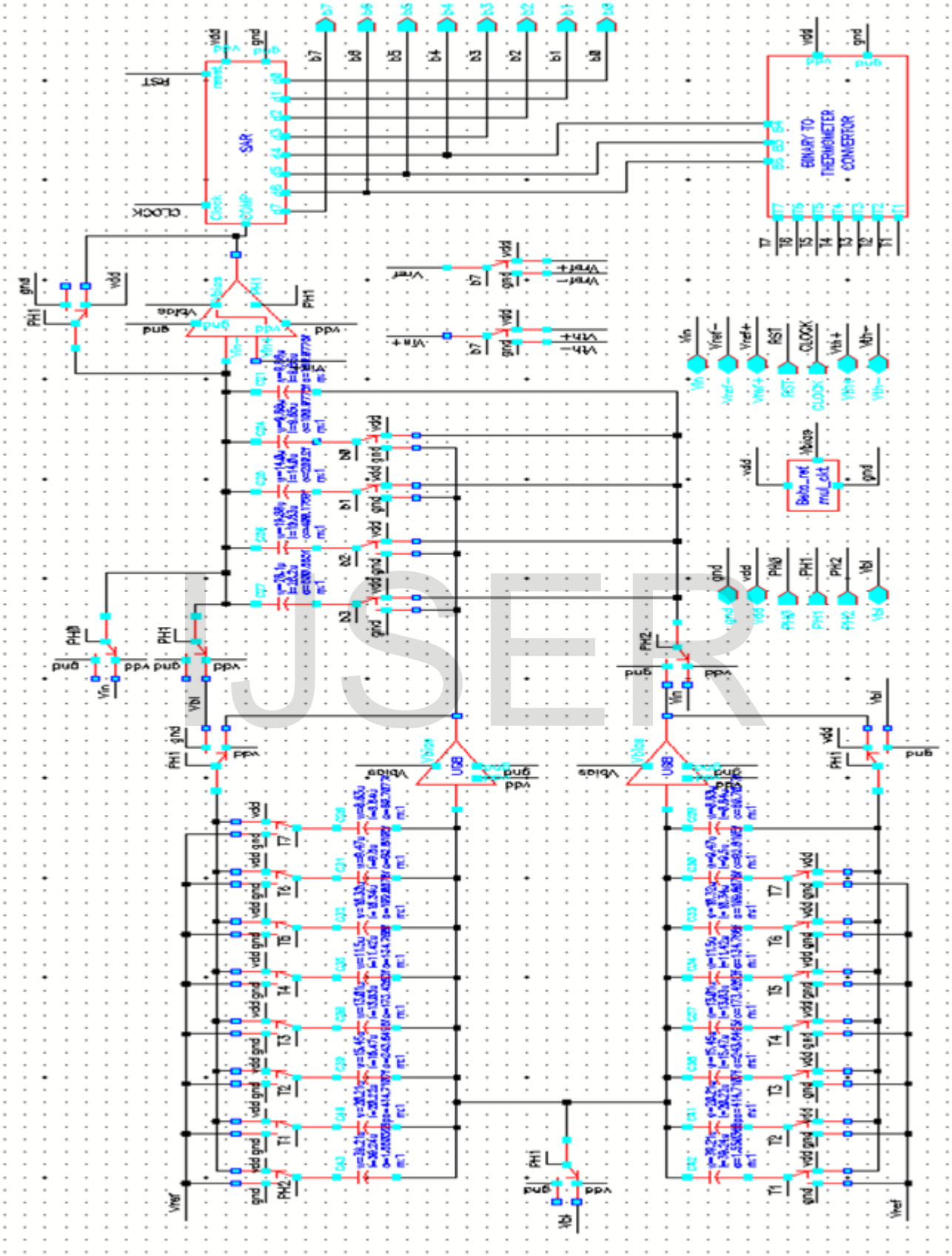


Figure 3: Circuit Diagram of two- step SARADC.

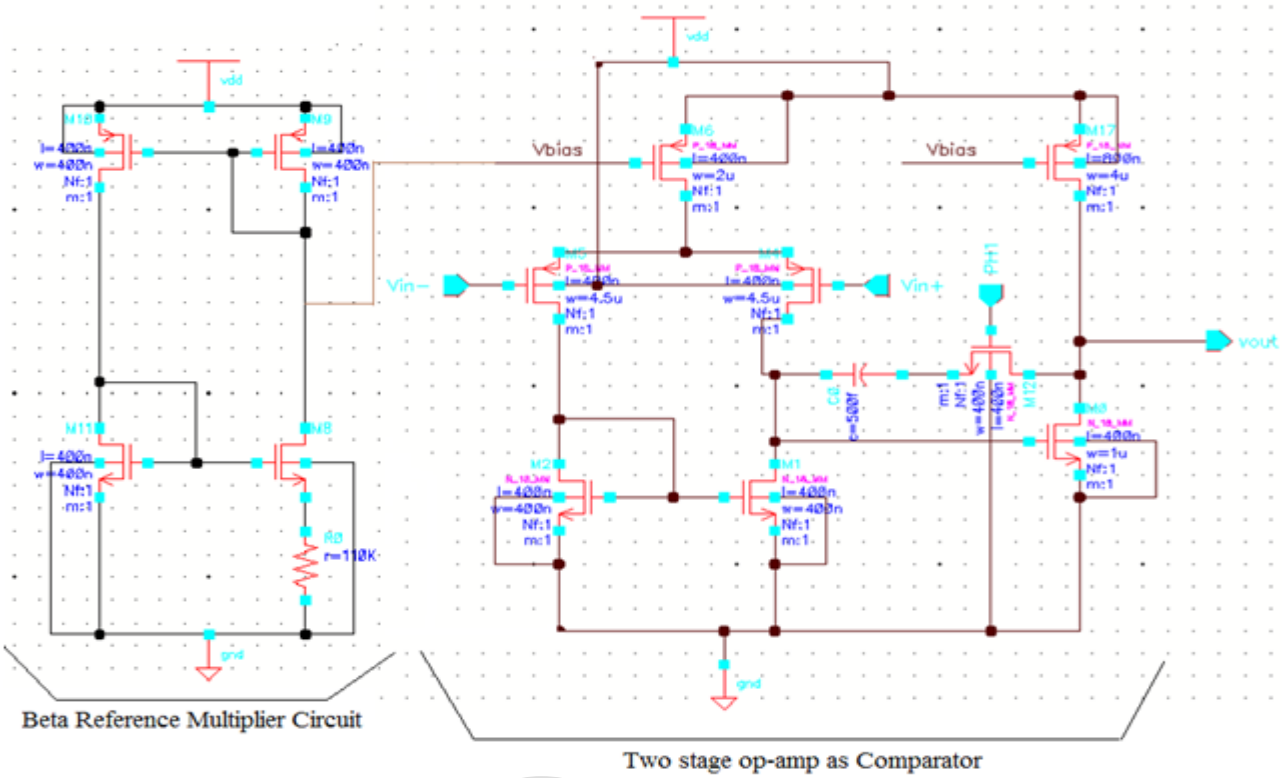


Figure 4: Circuit Diagram of Beta Reference Multiplier Circuit and Comparator.

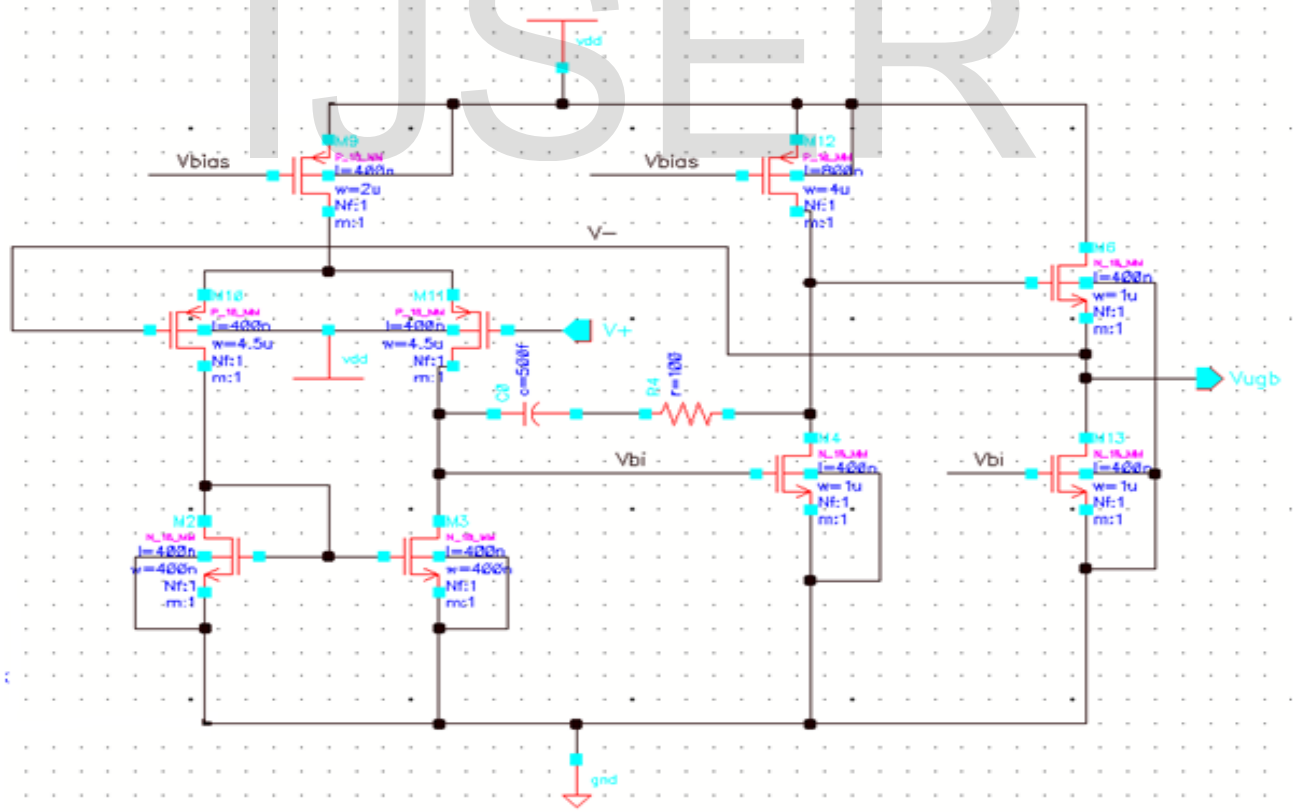


Figure 5: Circuit Diagram of Unity Gain Buffer.

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TABLE 1
SUMMARY OF SIMULATED RESULTS FOR COMPARATOR AND UGB

Specification	Value	
	Comparator	UGB
Gain (dB)	60.49	64.04
Unity Gain Bandwidth (MHz)	8.11	6.22
CMRR (dB)	59.26	63.28
PSRR (dB)	38.42	67.26
Slew Rate (V/µs)	7.61	3.83
ICMR (V)	1	1
Power Dissipation (µW)	9.27	13.91
Area (µm^2)	769.47	794.27

4 SIMULATION RESULTS

The neural signal is downloaded from internet [17]. A pwl file is created which can be used in cadence using analoglib> Vpwlf > path for pwl file. The standard deviation of the neural signal has been calculated and is found to be 42.6095 mV.

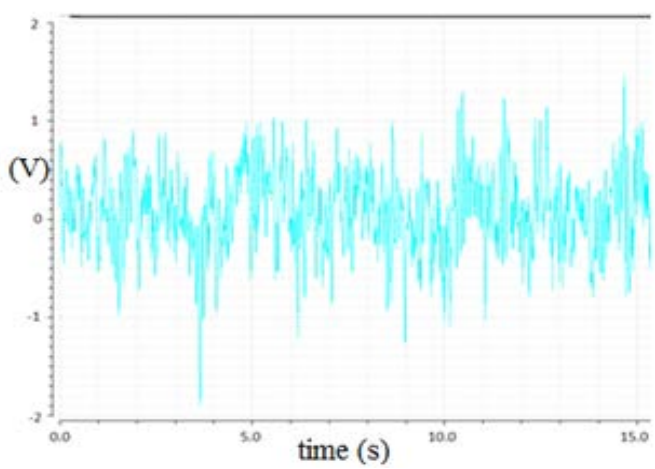

Figure 6: EEG Signal.

This signal is applied to the NLADC, the sampling frequency is 25KS/s, the output is shown in fig. 7; fig. 8 shows the transient power of NLADC.

Figure 7: Output Waveform of NLADC.

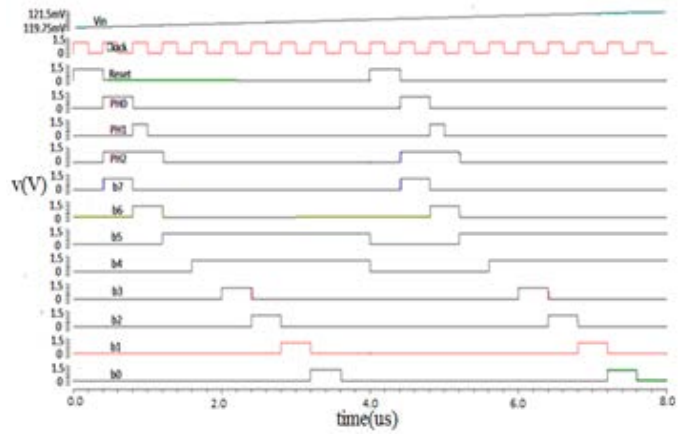

Figure 8: Transient Power of NLADC.

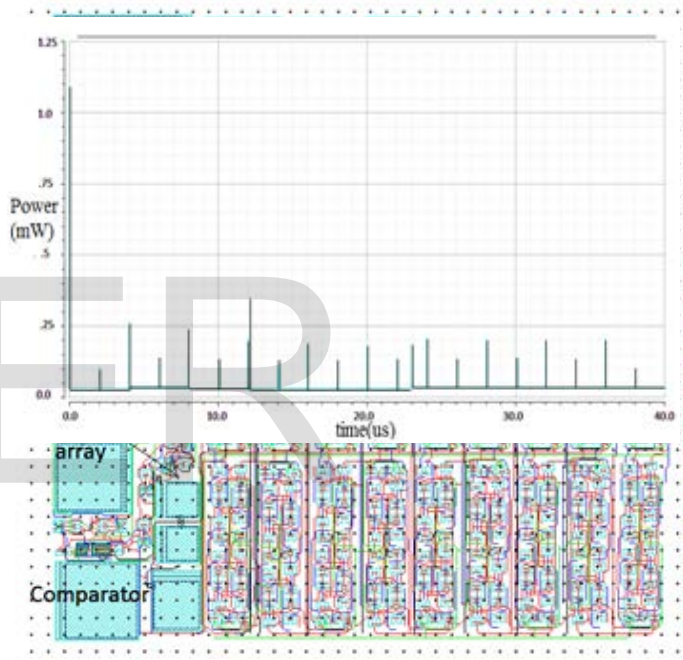

Figure 9: Layout of NLADC.

TABLE 2
SUMMARY OF SIMULATED RESULTS FOR NLADC

Specification	Value
Technology	0.18 µm
Supply Voltage	1.5V
Clock Frequency	250 KHz
Power Dissipation	31.04 µW
Area	0.03521 mm^2
Dynamic Range	64.1 dB

The dynamic range (DR) is calculated as it is done in [14], $Vlsb,_{min}$ is the minimum LSB size.

$$DR = (Vfs / Vlsb,_{\min}) \quad (5)$$

The dynamic range is calculated to be 64.1 dB. The capacitors designed in [18] are modified and basic building blocks of SAR logic are modified in this work. The layout is shown in fig. 9 and requires an area of 190.56 × 184.77 μm².

4 Conclusion

In this work the non-linear ADC for neural signal recording has been successfully designed and implemented in 0.18 μm technology with the supply voltage of 1.5 V. The maximum resolution achieved is 9.7 bits and the minimum resolution achieved is 2 bits which leads to bit rate reduction. The NLADC has 8 physical bits. The dynamic range is 64.1 dB, which is 15.9 dB higher than its linear counterpart. It occupies an area of 0.03521 mm² and power dissipation of 31.04 μW has been achieved.

The design is most advantageous for the neuroscientific studies where the loss of information is not preferred. This design can also be used as an integrated circuit in biomedical sensor front end. Another advantage of this design is that, it intentionally reduces the noise in the system.

The future work will optimize the design for particular applications. The focus of the current work was to design the NLADC for low power supply voltage in order to reduce power consumption. In the next implementation, several improvements could be made to the architecture to improve the power dissipation of the NLADC.

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